
VHDL Synthesis using Intel Quartus

In this exercise you will synthesize FPGA code for Lane detection for self-driving cars and test it using remote lab.

1. Download Intel Quartus Synthesis Software Lite Edition using this link:

<https://www.intel.com/content/www/us/en/products/details/fpga/development-tools/quartus-prime/resource.html>

2. Watch the tutorial Video “FPGA Vision -FPGA Remote Lab” by Prof. [Marco Winzker](#) to synthesize the lane detection VHDL code.

Link: <https://www.youtube.com/watch?v=H4WishN64TA>

VHDL Code Link: <https://github.com/Marco-Winzker/FPGA-Vision/tree/master/FPGA-Design>

3. Create an account to access Intel Cyclone V FPGA using this link:

<https://fpga-vision-lab.h-brs.de/weblab/invitation/1b69632240314530aa7d8a8e389cb1f2/register>

4. Login to your account using this link:

<https://fpga-vision-lab.h-brs.de/weblab/login>.

5. Upload the .sof file from the output_files folder in your project directory to the remote lab website.

↑ backup > Documents > Intelfpga > lane_detection > output_files

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Name	Date modified	Type	Size
lane.asm.rpt	9/20/2024 2:03 PM	RPT File	5 KB
lane.done	9/20/2024 2:03 PM	DONE File	1 KB
lane.eda.rpt	9/20/2024 2:03 PM	RPT File	6 KB
lane.fit.rpt	9/20/2024 2:03 PM	RPT File	245 KB
lane.fit.smsg	9/20/2024 2:03 PM	SMSG File	1 KB
lane.fit.summary	9/20/2024 2:03 PM	SUMMARY File	1 KB
lane.flow.rpt	9/20/2024 2:03 PM	RPT File	10 KB
lane.jdi	9/20/2024 2:03 PM	JDI File	1 KB
lane.map.rpt	9/20/2024 2:03 PM	RPT File	87 KB
lane.map.summary	9/20/2024 2:03 PM	SUMMARY File	1 KB
lane.pin	9/20/2024 2:03 PM	PIN File	33 KB
lane.sld	9/20/2024 2:03 PM	SLD File	1 KB
lane.sof	9/20/2024 2:03 PM	SOF File	2,385 KB
lane.sta.rpt	9/20/2024 2:03 PM	RPT File	138 KB
lane.sta.summary	9/20/2024 2:03 PM	SUMMARY File	2 KB


6. Upload an image of your choice and report the output image and the power consumption

FPGA Core Current:

36.95 mA

(Core Supply Voltage is 1.1 V)

<< < Select Input Image > >>



Choose File No file chosen

Upload your own input image now

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